C **0800CST203122004** **Pages: 2**

Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Examination December 2021 (2019 scheme)

Course Code: CST203

Course Name: Logic System Design

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1 Do the following base conversions (3)

a) $(96DE)_{16}$ to octal

b) $(1011011000)_2$ to octal

2 Subtract -12 from 23 using 2's complement representation and 1's complement representation (3)

3 State and prove extended De Morgan's theorem (3)

4 Using Huntington's postulates prove that (3)

a) x + x = x

b) x + 1 = 1

5 Distinguish between decoder and demultiplexer (3)

6 Design a half adder circuit from its truth table (3)

7 Distinguish between T flip-flop and D flip-flop (3)

8 Explain race around problem. How can it be eliminated? (3)

9 Write the algorithm for addition of two binary numbers in 2's complement form (3)

10 What is programmable logic array? Where is it useful? (3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 a) Convert i) $(214)_{10}$ to binary, octal, BCD and hexadecimal (4)

ii) (128) to binary, octal, BCD and hexadecimal (4)

b) Represent -219 and -114 in (6)

i) sign magnitude form ii) 1's complement form

iii) 2's complement form

12 a) Add 127 and 765 assuming the numbers are i) octal ii) BCD iii) hexadecimal (6)

b) Subtract 157 from 615 assuming the numbers are i) octal ii) BCD (6)

iii) hexadecimal iv) 2's complement form (2)

Module 2

13 a) Define Boolean algebra. Give an example (8)

b) Show that any digital circuit can be implemented using universal gates (6)

14 a) Simplify the Boolean function $F(a,b,c,d) = \sum (0,1,2,5,7,8,9,10,11,13,15)$ using K map (7)

b) Verify your answer using tabulation method. (7)

Module 3

15 a) Explain parallel adder/subtractor circuit with a logic diagram (8)

b) Design a carry look ahead adder circuit for four bit binary addition (6)

16 a) Design a code converter circuit for converting binary number to BCD number (8)

b) Design a 4x2 encoder circuit (6)

Module 4

17 a) Explain 3 bit binary asynchronous counter with a logic diagram and timing sequence (8)

b) Explain asynchronous BCD counter (6)

18 a) Explain i) SR flip-flop ii) JK flip-flop iii) master-slave flip-flop with excitation table and characteristic equation (12)

b) Explain edge triggered flip-flop (2)

Module 5

19 a) Explain a ring counter with a logic diagram, timing sequence and state diagram (10)

b) Explain with a logic diagram a serial in parallel out shift register (4)

20 a) Illustrate the algorithm for addition and subtraction of two BCD numbers with an example (8)

b) Explain with an example how simple functions can be implemented using PLA (6)

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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Examination December 2020 (2019 Scheme)

Course Code: CST203

Course Name: LOGIC SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1	Convert $(456.78)_{10}$ to a) binary b) octal and c) hexadecimal	(3)
2	Write a) 1's complement and 2) 2's complement representations of (-126)	(3)
3	State and prove De Morgan's Theorem	(3)
4	Design a circuit using NAND gates for implementing EXCLUSIVE-OR function	(3)
5	Design a half adder circuit using any universal gate.	(3)
6	Draw the logic diagram of a 2x1 multiplexer circuit	(3)
7	Derive the characteristic equation of a D flip flop from its excitation table.	(3)
8	How is a sequential circuit different from a combinational circuit? Give an example for each circuit.	(3)
9	Distinguish between a ring counter and Johnson counter	(3)
10	When do you implement a combinational circuit using ROM and when do implement a combinational circuit using PLA in preference to ROM.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	a) Convert i) $(13AF)_{16}$ to octal ii) $(10110101.101)_2$ to decimal	(6)
	b) Add i) BCD numbers 1567 and 968 ii) octal numbers 2376 and 5677	(8)
12	a) Perform the following operations using 2's complement representation i) (-34) + (+21) ii) (+26) – (-12) iii) (-33) + (-22) iv) (+45) – (+32)	(10)
	b) Convert i) (10011010) in 2's complement form to decimal ii) (10111001) in 1's complement form to decimal	(4)

Module 2

13	a) Using K Map simplify the function $F(w, x. y, z) = \sum (0,1,2,3,5,7,8,9,10,13,15)$	(8)
	b) Express the above function in product of maxterms form.	(6)

14 a) Using tabulation method simplify the function (8)

$F(w,x,y,z) = \sum (0,2,4,5,6,7,8,12,13,14,15)$

b) Express the following functions in a canonical form (6)

i) F= D+BC' ii) F= AB' +BC'

Module 3

15 a) Design a full subtractor circuit. (6)

b) Design a code converter for converting a BCD to excess-3 code. (8)

16 a) Explain BCD adder using a block diagram. (7)

b) Design a 2 bit magnitude comparator. (7)

Module 4

17 a) With a logic diagram explain how a master slave flip flop overcomes race around problem. (7)

b) Design a 2 bit synchronous counter. (7)

18 a) Draw the state diagram and logic diagram of a BCD ripple counter. (6)

b) Design a 3 bit synchronous up-down counter. (8)

Module 5

19 a) Explain the working of a 3 stage Johnson ring counter with a block diagram (7)

b) Explain the working of a 3 bit bidirectional shift register with parallel load. (7)

20 a) Illustrate the algorithm for addition and subtraction of two floating point numbers. (7)

b) Illustrate the algorithm for addition and subtraction two binary numbers in sign magnitude form. (7)

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